a trench network extending into said epitaxial region from an upper surface of said epitaxial layer and forming a plurality of mesas within said device;

a plurality of MOSFET cells that comprise: (a) a source region of said first conductivity type disposed within one of said mesas, (b) a body region of second conductivity type disposed within said one of said mesas, said body region forming a junction with said source region, (c) a drain region of first conductivity type at least partially disposed within said one of said mesas, said drain region forming a junction with said body region; and (d) a gate region situated within said trench network such that it is adjacent said source region, said body region and said drain region, said gate region comprising (i) an insulating region lining at least a portion of said trench network and (ii) a conductive region within said trench network adjacent said insulating region, said conductive region being separated from said source, body and drain regions by said insulating region; and

a plurality of Schottky dioide cells formed over bottom portions of said trench network, which Schottky dioide cells comprise a conductor portion that is in Schottky barrier rectifying contact with said epitaxial layer,

wherein at least some of said gate regions of said MOSFET cells are positioned along sidewalls of said trench network adjacent said conductor portions of at least some of said Schottky diodes.

**11**. The device of claim 10, wherein said conductor makes ohmic contact with said source regions and said body regions.

**12**. The device of claim 11, wherein said conductor comprises one or more of titanium tungsten, platinum silicide, aluminum and aluminum alloy.

**13**. The device of claim 10, wherein said gate region comprises a doped polysilicon region adjacent a silicon dioxide region.

**14**. The device of claim 10, wherein said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

**15**. The device of claim 10, wherein said semiconductor is silicon.

**16**. The device of claim 10, wherein at least some of said MOSFET cells and at least some of said Schottky diode cells are arranged in a geometric configuration selected from an in-line square geometry, an offset square geometry, and a hexagonal geometry.

**17**. The device of claim 10, wherein at least some of said MOSFET cells are octagonal cells.

**18**. The device of claim 10, wherein at least some of said MOSFET cells and at least some of said Schottky diode cells are arranged in a geometry comprising alternating first and second cell rows, wherein the cells of said first cell rows are greater in area than the cells of said second cell rows, and wherein said cells of said first cell rows are octagonal cells.

**19**. The device of claim 18, wherein said cells of said first cell rows are regular octagons.

**20**. The device of claim 18, wherein said MOSFET cells are positioned within said first cell rows and said Schottky diode cells are positioned within said second cell rows.

**21**. The device of claim 18, wherein said cells of said second cell rows are octagonal cells or square cells.

**22**. The device of claim 14, further comprising a heavily doped contact region for contact to the body region.

**23**. The device of claim 14, further comprising a p-type region that is below the Schottky diode and contacts the perimeter of the Schottky diode.

**24**. A merged device comprising Schottky diode cells and MOSFET cells, wherein

said Schottky diode cells are located at the bottom of a trench network, and

wherein certain gate regions of said MOSFET cells are provided on sidewalls of said trench network.

**25**. A method of forming a merged device comprising:

forming a plurality of Schottky diode cells; and

forming a plurality of MOSFET cells,

wherein said Schottky diode cells are located at the bottom of a trench network, wherein gate regions of said MOSFET cells comprise a conductive region and an insulating region, wherein certain of said gate regions are provided on sidewalls of said trench network, and wherein said conductive regions of said gate regions are formed without the aid of a masking layer.

**26**. The method of claim 25, wherein said gate conductors are formed by etching a doped polysilicon layer in an anisotropic etching process.

**27**. A method of providing a design for a merged device that comprises a plurality of Schottky diode cells and a plurality of MOSFET cells, said method comprising:

removing one or more source/body mesas within a trench MOSFET device design; and

locating one or more Schottky diode cells where the removed mesa was formerly located.

* * * * *